T.Rambabu, CH.Harikrishna / International Journal of Engineering Research and Applications (IJERA)
ISSN: 2248-9622 www.ijera.com
Vol. 1, Issue 4, pp. 1511-1514

HARMONIC ELIMINATION OF CASCADED MULTILEVEL INVERTER FOR MEDIUM-VOLTAGE APPLICATION

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***ABSTRACT*—In this paper, a low-frequency square-wave inverter with a series-connected pulse width modulation (PWM) inverter is investigated for high-power applications. The series compensators produce only the desired harmonic voltages to make the net output voltage sinusoidal with small PWM switching harmonics only. An open-loop control strategy for the series compensator is proposed in this paper. This strategy indirectly sets the compensator dc bus voltage to the desired level. No external dc source or active power at fundamental frequency is required to control this dc bus voltage. Different variations of this basic strategy are presented in this paper for medium-voltage applications. Theoretical analysis of this strategy is presented in this paper with simulation and experimental results.**

***Index Terms*—AC motor drives, power conversion, power conversion**

I. INTRODUCTION

THE THREE-PHASE two-level pulse width modulation (PWM) inverter is a highly preferred scheme as a voltage source inverter for various applications. To make this inverter output voltage sinusoidal, a simple *L–C* filter is normally introduced at the output of this PWM inverter. For high-power applications, the switching frequency of the two-level inverters is very much restricted due to the limitation of the available power devices. This introduces increased harmonic current at the load. It also demands bigger size of the *L–C* filter to obtain sinusoidal voltage at the output. For special applications like high-speed motor drive, where the fundamental base frequency of the voltage source can be as high as 1 kHz, PWM control of the inverter is a difficult proposition. This is again due to the limitation of the switching devices like insulated-gate bipolar transistors (IGBTs).These problems are tackled by various multilevel topologies most of them require Separate dc voltage source for each inverter cell. Proposes a method to draw active power at fundamental frequency by each cell to regulate its dc bus voltage. a high-frequency PWM inverter is connected in series with a low-frequency square-wave inverter. Both the inverters require separate dc sources. In this paper, a variant of series-connected converters and its control strategy are proposed for sinusoidal output. The basic three-phase high-voltage inverter works in square-wave made as in but the series-connected inverters produce only the harmonic voltages using carrier-based PWM strategies, unlike all other papers mentioned before.

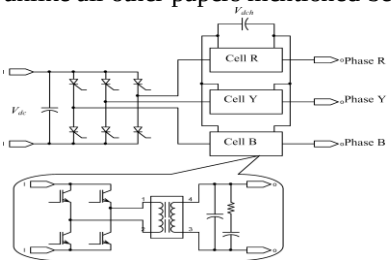

Fig. 1. Basic converter topology.

II. FUNDAMENTALS OF THE PROPOSED INVERTER TOPOLOGY AND CONTROL

The proposed topology has evolved from the typical series compensating devices like the unified power quality conditioner (UPQC),digital video recorder (DVR), etc. The main Square-wave inverter is solely responsible for the fundamental voltage. Each phase has series-connected single-phase inverter that produces only the required harmonic voltages.These three single-phase cells normally have common dc bus voltage.
Usually, the value of this common dc bus voltage is less than that of the main square-wave inverter.

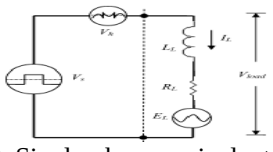

Fig. 2. Single-phase equivalent circuit of the proposed converter and the load.

PWM mode of operation of the series inverter [This common dc bus voltage has to be generated separately. Alternatively, a small amount of controlled

active power has to be drawn by the series inverters to control this dc bus voltage the desired harmonic voltages are injected to the line using three single phase transformers, as shown above Small capacitor and resistor networks at the output of the single-phase transformers remove the switching harmonics.

In this paper, natural open-loop control of this series compensator dc bus voltage is proposed without drawing any active power at fundamental frequency. A separate active dc voltage source is also not required here. The active power drawn at harmonic frequencies regulates the dc bus voltage of the series compensator. The basic philosophy of the operation is established shortly

A per-phase equivalent circuit of this proposed system is shown in Fig. 2. The load could be a motor with equivalent leakage impedance *RL, LL* , and the sinusoidal back emf *EL* at fundamental frequency. It may also represent the grid voltage *EL* at fundamental frequency and the series impedance *RL* and
LL . The square-wave voltage varies from +*V*dc/2 to −*V*dc/2, with the time period of 2*π*/*ωf* . Mathematically, it can be expressed
using the unit step function *u*(*t*) as follows:

VS (t) = ∑[***Vdc{u(t-2nπ/wf)}]***

Vdc/2= +-1= +-2= +-3

Here, *V*dc is the dc bus voltage of the square-wave inverter and *ωf* is the fundamental frequency (in radians per second) of the square wave. Using Fourier analysis, the desired series Compensator output voltage can now be obtained as

Vh (t)= ∑[4 ***Vdc/2/ nπ*** sinn ***wf*** *t*)

, where "*n*" is odd number.

After perfect compensation using series converter, the load voltage becomes

*V*load (*t*)= ∑[4 ***Vdc/2/ nπ*** sinn ***wf*** *t*)

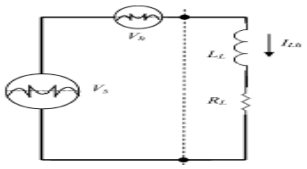

Fig. 3. Single-phase equivalent circuit of the harmonic voltages only.

Now, the peak value of the series compensator output voltage is *V*dc/2. This can be seen by subtracting (3) from (1). Thus, the minimum dc bus voltage required for the series compensator is *V*dc/2. In the proposed topology, there is no separate source to maintain this desired value of the series compensator dc bus voltage. Let us assume that the modulation depth (*m*) of the *n*th harmonic component of the series compensator is as follows:

$$m = 4/n\pi \quad . (4)$$

Therefore, the output *n*th harmonic component of the series compensator is as follows:

$$V_{nh}(t) = m\,V_{\mathrm{dch}}(t)\,\sin(n\omega_f t) = \frac{4\,V_{\mathrm{dch}}(t)}{n\pi}\,\sin(n\omega_f t). \quad (5)$$

Here, *V*dch(*t*) is the dc bus voltage of the series compensator at any time *t*. The *n*th harmonic equivalent circuit of this converter with load is shown in Fig. 3. Assuming that the dynamics of
*V*dch(*t*) is very slow, the average active power *Pnh* absorbed by the series compensator due to the *n*th harmonic

$$P_{nh} = \frac{1}{2}\left(\frac{4}{n\pi}\right)^2 \frac{((V_{\mathrm{dc}}/2) - V_{\mathrm{dch}}(t))}{R_L^2 + (n\omega_f L_L)^2} V_{\mathrm{dch}}(t)\,R_L. \quad (6)$$

Neglecting the losses of the dc bus capacitor, the dynamical equation of *V*dch(*t*) can now be written as follows:

$$3\sum_{n=5}^{\infty} P_{nh} = V_{\mathrm{dch}}(t)\,C_h \frac{dV_{\mathrm{dch}}(t)}{dt}. \quad (7)$$

Here,*Ch* is the total dc bus capacitor of the series compensator and Σ*n*=5 *Pnh* is the net active power considering all three phases. It has to be noted that all the triple harmonics like third, ninth, etc., will not contribute any power since there is no neutral connection (Fig. 1). Using (6) and (7), the dynamics of *V*dch(*t*) becomes

IV. PRACTICAL ISSUES OF LOSSES IN THE SERIES COMPENSATORS

The analysis presented in the earlier sections is assumed have zero losses in the series compensator. However, the practical converters have the switching and the conduction losses. An approximate equivalent circuit of each harmonic cell is shown in In steady state, the series compensator current is mostly dominated by the fundamental component of current. This is represented by a current source *IS* sin (*ωf t*) In this equivalent circuit, the *V*CE(sat) (or *V*F) drop of the IGBT switches (or the anti parallel diodes) can be approximately represented
by a square-wave voltage signal whose fundamental frequency is same as that of the series compensator current. This square-wave voltage is also in phase with the series compensator current *IS* sin (*ωf t*). In case of a MOSFET-based compensator, the drain resistances (*Rd*) can be represented as shown in Fig. 8. Now, the actual switches shown in Fig. 8 have only the non ideal switching's but no conduction drops. For ideal switching,

the voltage at port *a–b* (*V*ab) in Fig. 8 is mainly *mV*dch sin (*nωf t*) and the switching harmonics. Therefore, there is no net active power transfer across the port *a–b*. Hence, the current source, i.e., the main square-wave inverter delivers the complete conduction losses of each harmonic cell. Due to non ideal switching's, *V*ab has the additional harmonic components of "*nωf* " and a small amount of voltage having frequency
ωf due to the current source. This small voltage also is in phase with this current source *IS* sin (*ωf t*). Therefore, there is a small amount of net active power transfer from the current source, i.e., the main square-wave inverter to the compensator across this port *a–b*.This small active power shares the switching losses of the compensator. Depending upon the device switching characteristics, the compensator dc bus *V*dch also shares the switching losses. Moreover, half of the total switching per fundamental
cycle (1/*ωf*) is soft switching (ZVS). Therefore, the net power loss (*P*sw) at the compensator dc bus (*V*dch) consists of small amount of device switching power loss only. Thus, a small amount of active power is required to be drawn by this compensator to maintain its dc bus voltage *V*dch in steady state. For the simplification, this switching power loss (*P*sw) can be assumed to be proportional to *V*dch. In steady state, *P*sw should be equal to the active power due to *n*th harmonic for *n*th harmonic cell (*Pnh*). Using (11), the steady-state dc bus voltage
*V*dch of the *n*th harmonic cell can be written as

$$Ksw\ Pnh = 1/2(\ 4/\ n\pi)\ 2\ \frac{((Vdc/2) - Vdch\ (t))\ R2L}{R2L + (n\omega f\ LL\ )2\ Vdch}$$

Where Ksw is the proportionality constant. For standard designed converter, *P*sw is very small,
and hence, *K*sw is also negligibly small. Then, *V*dch is slightly less than the desired voltage 2*V*dc/*nπ*. Therefore, this compensator loss introduces a small amount of uncompensated *n*th harmonic voltage at the load terminals. For a standard designed converter, this small loss does not lower the performance of the series compensator appreciably, as evident from the experimental results presented later. , it can be seen that the performance of the compensator deteriorates for the higher order harmonics. Since the higher order harmonics have the lower order magnitudes this may not be a serious limitation of this configuration.

Simulinkmodel for overall system

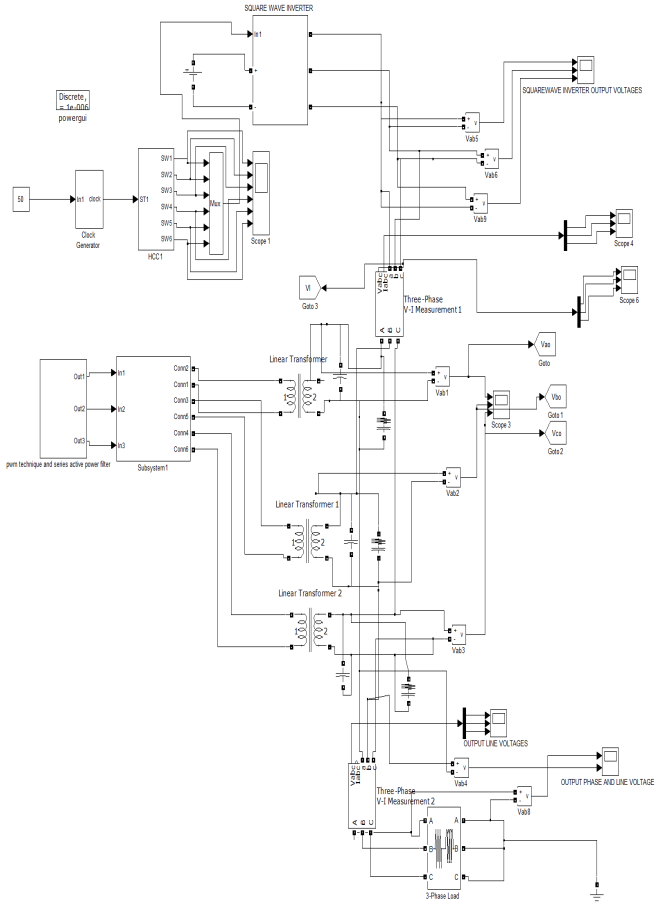

Fig 4.simulation diagram

V. SIMULATION RESULTS

The proposed strategies are simulated to validate the performances. Fig1 line to line voltage of Square Wave Inverter

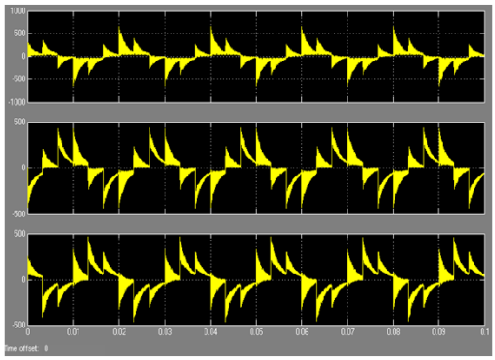

Fig 5 . Injected Harmonic Voltages

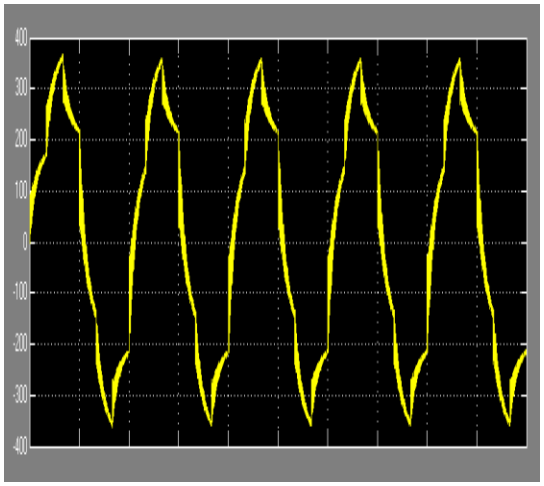

Fig 6. Out put phase Voltage

VII. CONCLUSION

In this paper, an open-loop natural control of voltage source inverter has been proposed mainly for high-power applications. The main square-wave inverter is built with high-voltage low switching- frequency semiconductor devices like integrated gate commutated thyristors (IGCTs). The series compensators are IGBT-based inverters and operate from relatively low dc bus voltages at high switching frequencies. The series compensators produce only the desired harmonic voltages to make the net output voltage sinusoidal. For medium-voltage application, several compensating PWM inverters are connected in series. Each cell compensates one particular harmonic only. As the order of harmonics increases, the required dc bus voltage level drops. This enables to exploit higher switching frequency for higher order harmonic cell. It has been established both theoretically and experimentally that the dc bus of the compensators do not require any external dc source or closed-loop controller for this proposed strategy. The active power at harmonic frequencies keeps the compensator dc bus voltage charged. For variable-speed drives applications, the magnitude of the fundamental output voltage should be controlled by regulating the dc bus voltage of the square-wave inverter. For static synchronous compensator (STATCOM) applications, the limited variation of this dc bus voltage may also be required. This can be achieved by drawing small active power at fundamental frequency from the grid

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